WHAT IS CLAIMED IS:

1. A data processing device including a set-associative cache memory capable of performing associative operation using tag information for an indexed cache line, said cache memory comprising:

way prediction means for performing way selection based on the prediction in parallel with the associative operation;

generation means for generating way selection determining information based on the associative operation using the subsequent access address during a penalty cycle caused by a prediction miss of said way prediction means; and

control means for making a way selected for the subsequent access address after the penalty cycle on the basis of the way selection determining information.

2. The data processing device according to claim 1, wherein said control means makes a way selected on the basis of the way selection determining information instead of the prediction by said way prediction means.

3. The data processing device according to claim 1, wherein said control means controls rewriting of prediction result information obtained by said way prediction means and corresponding to the way selection determining information.

4. A data processing device including a set-associative cache memory capable of performing

associative operation using tag information for an indexed cache line, said cache memory comprising:

instruction means for switchably instructing either of a first operation mode for making a way selection according to the result of the associative operation and a second operation mode for making a way selection based on the prediction in parallel with the associative operation.

5. The data processing device according to claim 4, further comprising a CPU connected to said cache memory, wherein said instruction means is register means accessible by said CPU.

6. The data processing device according to claim 1, wherein the associative operation is to compare predetermined address information contained in access address information with the tag information for each way of the indexed cache line and generate an association result signal indicative of an association hit or association miss on a way basis.

7. The data processing device according to claim 1, wherein the prediction by said way prediction means is processing for determining the least previously selected way as a selected way on the basis of way selection history information for each cache line.

8. A data processor including a set-associative cache memory capable of performing associative operation using tag information for an indexed cache line, and a CPU connected to the cache memory, said cache

memory comprising a plurality of way and cache control means, wherein

said cache control means makes a way selection based on the prediction in parallel with the associative operation in response to the access operation of said CPU, generates way selection determining information during a penalty cycle caused by a prediction miss or cache miss, in which a predictively selected way does not match the result of the associative operation, on the basis of the associative operation using the subsequent access address, and performs control for making a way selected for the subsequent access address after the penalty cycle on the basis of the way selection determining information.

9. The data processor according to claim 8, wherein said cache control means makes a way selected on the basis of the way selection determining information instead of the prediction by said way prediction means.

10. The data processor according to claim 8, wherein said cache control means controls rewriting of prediction result information obtained by said way prediction means and corresponding to the way selection determining information.

11. The data processor according to claim 8, wherein said cache control means issues an instruction of an external memory access to the subsequent access cache miss during the penalty cycle caused by the

prediction miss.

12. The data processor according to claim 8, wherein said cache control means includes storage means for storing way selection history information on a cache line basis, and the history information is information for determining a way corresponding to the least recently accessed information as a selected way.

13. The data processor according to claim 8, wherein said cache control means updates the history information so that the latest access way selected from the indexed cache line can be specified in a prediction process to be performed later.

14. The data processor according to claim 8, wherein said cache control means reads out the history information from said storage means according to the address information for indexing the cache line to perform a predictive selection of a way based on the read-out history information.

15. The data processor according to claim 8, wherein said cache control means judges, on the basis of the tag information contained in the indexed cache line, whether a cache miss or prediction miss occurs in the way selection process, reselects a way in response to a cache hit and the judgment result of a prediction miss while updating the history information corresponding to the cache line to be accessed, and instructs an external access in response to the judgment result of the prediction miss so that the cache line to be

accessed will be replaced while updating the history information corresponding to the cache line to be replaced.

16. The data processor according to claim 8, wherein said data processor is formed on a semiconductor chip.